Claims:

1. A method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising:

depositing a barrier and seed layer within a trench formed in the semiconductor wafer;

generating, in response to deposition results, first control parameters;

performing electrochemical plating to deposit a copper layer upon the barrier and seed layer;

generating, in response to plating results, second control parameters;

polishing upon the copper layer;

generating, in response to polishing results, third control parameters; and

controlling at least one of the polishing process in response to the first control parameters or the deposition process in response to the third control parameters.

2. The method of claim 1 further comprising:

etching the trench into the semiconductor wafer;

testing a trench geometry;

generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and

using the fourth control parameters to process the semiconductor wafer having the trench geometry.

3. The method of claim 1, wherein the step of controlling the polishing process comprises:

controlling at least one of control radial pressure profile and the rotational speed of the polishing pad in response to at least one of the first, second or third control parameters.

4. The method of claim 1, wherein the step of controlling the polishing process further comprises:

setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first, second or third control parameters.

5. The method of claim 1, wherein the step of controlling the depositing process further comprises:

controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters.

6. The method of claim 1, wherein the step of controlling the depositing process further comprises:

controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters.

7. The method of claim 1, wherein the step of controlling the plating process further comprises:

controlling at least one of electroless thickness, patch thickness, current or pulse sequence, or additives to compensate for at least one of voids or planarization issues.

8. The method of claim 1 further comprising:

obtaining gap fill information.

9. The method of claim 8 further comprising:

tuning plating parameters of subsequently plated wafers in response to the gap fill information.

10. The method of claim 9, wherein the step of tuning plating parameters further comprises:

controlling at least one of current density, rotation speed, and anode to wafer distance in response to the gap fill information.

11. The method of claim 8 further comprising:

tuning polishing parameters of the wafer in response to the gap fill information.

12. The method of claim 1 further comprising:

tuning processing parameters of subsequently process wafers in response to the control parameters.

13. The method of claim 1, wherein at least one of the results utilized to generate the control parameters are selected from the group consisting of barrier seed step coverage of a trench and via having a specific size aspect ratio, gap fill, void detection, planarization, dishing, erosion, copper thickness, trench depth, dielectric constant, residual metal on a comb structure, via or snake open in a standard structure based on a voltage contrast or two-probe measurement, barrier thickness, copper seed thickness, copper thickness, copper bulk resistance, dielectric thickness, dielectric constant, presence of particles, presence of residue and systematic process defects.

14. A method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising:

depositing a barrier and seed layer within a trench formed in the semiconductor wafer;

testing a barrier and seed layer thickness;

generating, in response to the barrier and seed layer thickness, first control parameters for the electrochemical plating tool and the barrier and seed layer deposition tool;

performing electrochemical plating to deposit a copper layer upon the barrier and seed layer in accordance with the control parameters;

testing at least one of copper thickness and resistivity;

generating, in response to the testing at least one of copper thickness and resistivity, second control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool;

performing chemical-mechanical polishing upon the copper layer in accordance with the second control parameters;

testing a copper uniformity and residue of the polished semiconductor wafer;

generating, in response to the copper uniformity and residue, third control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool;

using the third control parameters in processing subsequent semiconductor wafers.

15. The method of claim 14 further comprising:

etching the trench into the semiconductor wafer;

testing a trench geometry;

generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and

using the fourth control parameters to process the semiconductor wafer having the trench geometry.

16. The method of claim 14, wherein the step of controlling the chemical-mechanical polishing tool further comprises:

setting at least one of control radial pressure profile and the rotational speed of the polishing pad in response to at least one of the second or third control parameters.

17. The method of claim 14, wherein the step of controlling the chemical-mechanical polishing tool further comprises:

setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first or third control parameters.

18. The method of claim 14, wherein the step of controlling the deposition tool further comprises:

controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters.

19. The method of claim 14, wherein the step of controlling the deposition tool further comprises:

controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters.

20. The method of claim 14, wherein the step of controlling the electrochemical plating tool further comprises:

controlling at least one of electroless thickness, patch thickness, current or pulse sequence, or additives to compensate for at least one of voids or planarization issues.

21. The method of claim 14 further comprising:

obtaining gap fill information.

22. The method of claim 21 further comprising:

tuning plating parameters of subsequently plated wafers in response to the gap fill information.

23. The method of claim 22, wherein the step of tuning plating parameters further comprises:

controlling at least one of current density, rotation speed, and anode to wafer distance in response to the gap fill information.

24. The method of claim 21 further comprising:

tuning polishing parameters of the wafer in response to the gap fill information.

25. A method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising:

depositing a barrier and seed layer within a trench formed in the semiconductor wafer;

generating, in response to deposition results, first control parameters;

performing electrochemical plating to deposit a copper layer upon the barrier and seed layer;

polishing upon the copper layer; and

controlling the polishing process in response to the first control parameters.

26. A method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising:

depositing a barrier and seed layer within a trench formed in the semiconductor wafer;

performing electrochemical plating to deposit a copper layer upon the barrier and seed layer;

polishing upon the copper layer;

generating, in response to polishing results, first control parameters;

and

controlling the deposition process in response to the first control parameters.

27. Apparatus for monitoring and controlling a multi-step semiconductor wafer processing system comprising:

a plurality of independently operating processing tools;

at least one metrology station for testing a semiconductor wafer after one or more process steps are performed by the plurality of independently operating processing tools;

a metrology data analyzer for analyzing data produced by the at least one metrology station and producing control parameters for said plurality of independently operating processing tools;

a plurality of process controllers for selectively applying the control parameters to the plurality of independently operating processing tools.

28. The apparatus of claim 27 wherein said at least one metrology station performs blanket and patterned wafer tests.

29. The apparatus of claim 27 wherein the independently operating processing tools comprise one ore more of: etch chamber, chemical-mechanical polishing tool, electrochemical plating cell, a physical vapor deposition chamber and a chemical vapor deposition chamber.

30. The apparatus of claim 27 wherein the multi-step semiconductor wafer processing system produces a copper interconnect using independently operating processing tools comprising: a barrier and seed layer deposition tool, an electrochemical plating cell and a chemical-mechanical polishing tool.